BYD Microelectronics Co., Ltd.

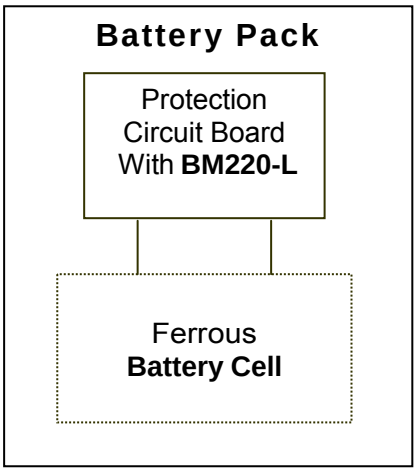
BM220-L Series

Two-cell Fe Battery Protectors

General Description

The BM220-L series are protection ICs for ferrous rechargeable battery packs. It includes voltage detection unit, voltage reference unit, bias unit, delay unit, and logic circuits. The BM220-L series have cell-balance function and high-accuracy voltage detection for protecting Two-cell ferrous battery packs from overcharge, over-discharge, excess-current and short circuit.

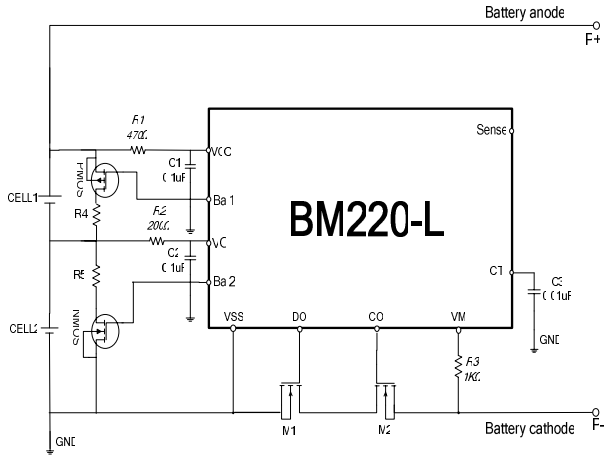
Applications



Features

- **Overcharge Threshold**
  - 3.600~ 4.000V
  - Accuracy ±50mV (25℃) ±80mV (-20℃~70℃)
- **Over-discharge Threshold**
  - Typ. 2.00V
  - Accuracy ±80mV
- **Balance Threshold**
  - Typ. 3.62V
  - Accuracy ±0.10V
- **Excess Current 1 Protection Threshold**
  - Typ. 0.20V @ VC = 2.85V, VCC = 5.70V
  - Accuracy ±0.02V
- **Excess Current 2 Protection Threshold**
  - Typ. 0.60V @ VC = 2.85V, VCC = 5.70V
  - Accuracy ±0.10V
- **Short Circuit Protection Threshold**
  - Typ. 1.50V @ VC = 2.85V, VCC = 5.70V
  - Accuracy ±0.50V
- **Low power consumption**
  - Typ. 10.0uA @ VC = 3.30V, VCC = 6.60V (Standard working current)
  - Typ. 0.90uA @ VC = 1.50V, VCC = 3.0V (Standby current)
- **Output Delay of Overcharge**
  - Typ. 85ms (connect a 0.01uF cap to CT)
- **Output Delay of Over-discharge**
  - Typ. 24ms @ VC = 1.90V, VCC = 3.80V

Typical Application Circuits



Recommended value:

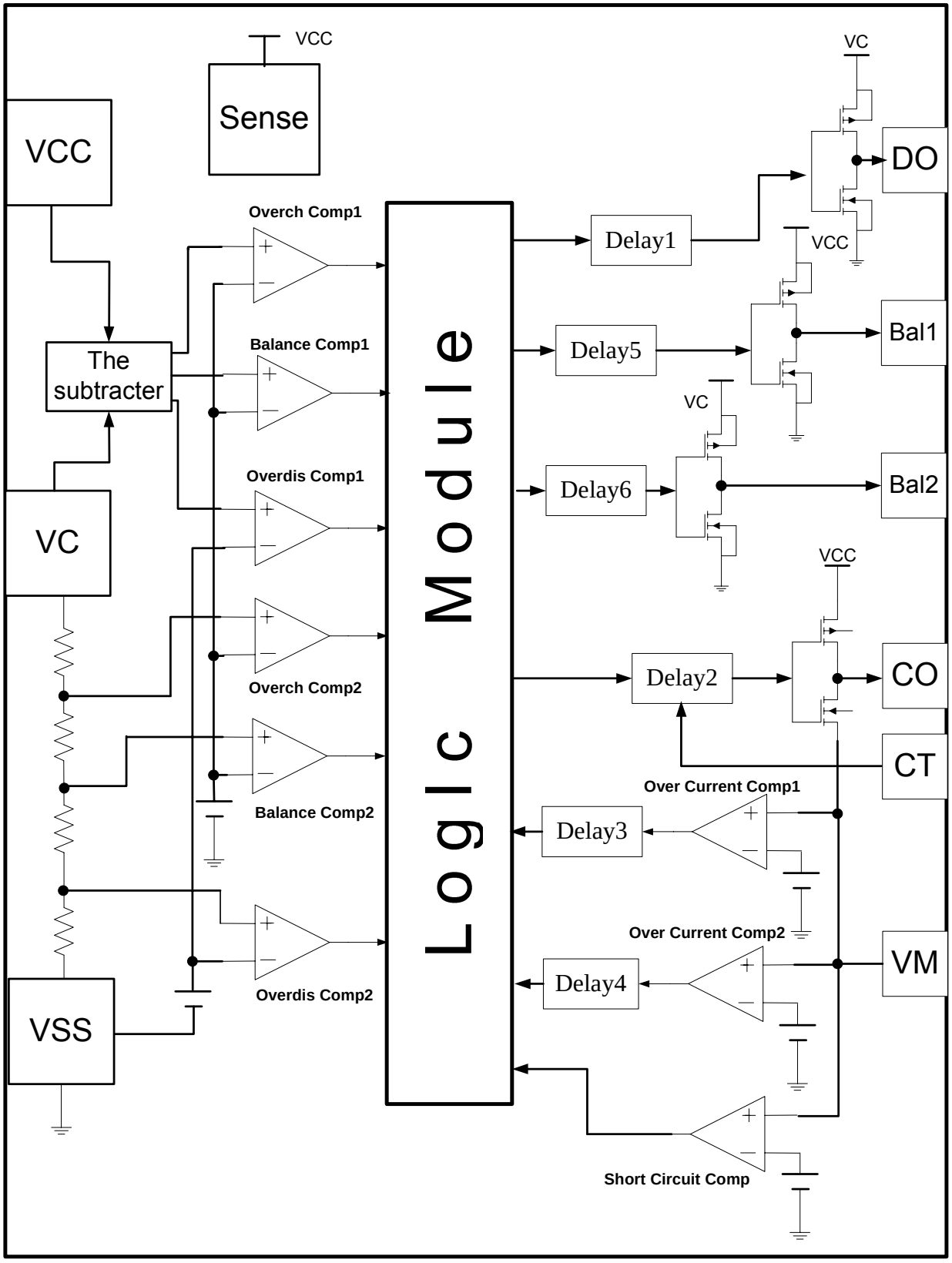
R_1=470Ω; R_2=200Ω; R_3=1KΩ;C_1=C_2 =0.10uF; C_3=0.01uf;

Notes

R_1C_1, R_2C_2 are to stabilize the supply voltage of the BM220-L series. R_1C_1 is hence regarded as the time constant for VCC pin. R_2C_2 is hence regarded as the time constant for VC pin. R_1 and R_3 can also be a part of current-limit circuit for the BM220-L series. Recommended values of these elements are as follows:

- R_2＜470Ω. A larger value of R_2 results in high detection voltage, low detection accuracy.
- R_3＜2.50kΩ. A larger value of R_3possibly counteracts resetting from over-discharge even with a charger.
- R_4, R_5 is determined by your balance bypass current.
- R_1+R_3≥1. 2kΩ. Smaller values may lead to power consumption over the maximum dissipation rating of the BM220-L series.

Block Diagram



Selection Guide

- **Type Number**

BM220-L-XX

Symbol	Meaning	Description
XX	Overcharge/Over-discharge detection threshold and accuracy	Assigned from AA to WW

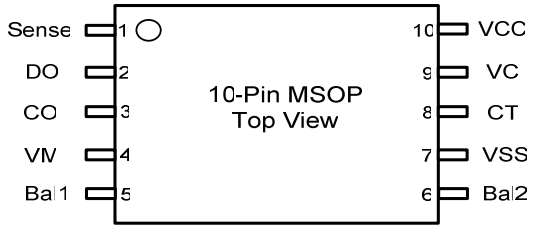
- **Type Number Option**

Through choosing the "XX", the Overcharge Detection Threshold Voltage (VCT1,2) , the Over-discharge Detection Threshold voltage (VDT1,2), and their accuracy of BM220-L can be decided.

Table 1. VCT1,2 & VDT1,2 & Marking (@ 25℃)

Type Number	VCT1,2	VCT1,2 Accuracy	VDT1,2	VDT1,2 Accuracy	Mark
BM220– L–FM	3.850 V	±50 mV	2.000 V	±80mV	220LM

Package Type



Pin Description

Pin number	Pin name	Description
1	Sense	Connect to VCC
2	DO	Over-discharge detection pin, CMOS output
3	CO	Overcharge detection pin, CMOS output
4	VM	The excess-current detection pin
5	Bal1	The balance control pin of cell1.
6	Bal2	The balance control pin of cell2.
7	VSS	Ground
8	CT	To connect capacitor for Overcharge detection delay
9	VC	The middle pin between two cells (to connect cell 1 cathode and cell 2 anode)
10	VCC	Positive power input pin (to connect cell 1 anode)

Function Description

1· Normal Condition:

When both VC and (VCC-VC) are between the Over-discharge Detection Threshold Voltage (VDT) and the Overcharge Detection Threshold Voltage (VCT), and the VM pin voltage between the Charger Detection Threshold Voltage (VCHA) and the Excess Current 1 Detection Threshold Voltage (VIT1), the outputs of DO pin and CO pin are on high level, making the charge and discharge MOSFETs on. Charging and discharging can be carried out freely.

2· Overcharge Condition:

During charging, when VC or (VCC－VC) increases higher than VCT and takes the Overcharge Detection Delay Time (T_{CT}) or longer, the output of CO pin will change from high level to low level, turning off the charging control FET to stop charging.

3· Overcharge Protection Release Condition:

The output of CO pin will change to high level, making charging recovered, when either of the following conditions come into being: (1) both VC and (VCC－VC) become lower than the Overcharge Release Voltage (VCR); (2) a load connects to VCC after a charger is disconnected from the battery pack, and both VC and (VCC－VC) are lower than VCT.

4· Over-discharge Condition:

During discharging, when VC or (VCC－VC) decreases lower than VDT and taking the Over-discharge Detection Delay Time (T_{DT}) or longer, the output of DO pin will change from high level to low level, turning off the discharging control FET to stop discharging.

5· Over-discharge Protection Release Condition:

The output of DO pin will change to high level, making discharging recovered, when either of the following conditions come into being: (1) a charger is connected to the battery pack, and the battery supply voltage becomes higher than VDT, and VM is higher than the Charger Detection Threshold Voltage (VCHA); (2) both the VC and (VCC－VC) become higher than the Over-discharge Release Voltage (VDR) and VM is between VCHA and VIT1.

6. Excess Current 1 Protection:

During discharging, the current varies with load, and VM increases with the rise of the discharging current. Once VM rises higher than the Excess Current 1 Detection Threshold Voltage (VIT1) and stays longer than the Excess Current 1 Detection Delay Time (T_3), DO pin changes from high to low level, turning off the discharging control FET. Once that excess current state is removed, i.e. VM＜VIT1, and the circuit recovers to normal state.

7. Excess Current 2 Protection:

During discharging, the current varies with load, and VM increases with the rise of the discharging current. Once VM rises higher than the Excess Current 2 Detection Threshold Voltage (VIT2) and stays longer than the Excess Current 2 Detection Delay Time (T_4), DO pin changes from high to low level, turning off the discharging control FET. Once that excess current state is removed, and VM＜VIT1, and the circuit recovers to normal state.

8. Short Circuit Protection:

This function has the same principle as the excess current protection. But, the delay time T_5 is far shorter than T_3 and T_4, and the threshold VSHORT is far higher than VIT1 and VIT2. When the circuit is shorted, VM increases rapidly. Once VM ≥ VSHORT, DO pin switches to low, turning off the discharging control FET. After the short circuit state is removed, and VM＜VIT1, the circuit recovers to the normal state. The short circuit peak current is related to VSHORT and the ON resistance of the two FETs in series.

9. Cell-balance Function: The cell-balance function is used to balance the two cells' voltage in the pack. When the (VCC-VC) is between the Cell-balance1 Threshold (VBAL1) and the Overcharge Detection Voltage(VCT), and VC is below the Cell-balance 2 Threshold (Vbal2) for the Cell-balance 1 Detection Delay

Time(T_{BAL1}) or longer, the Bal1 pin controls the P-MOSFET to switch on the bypass balance circuit. When the (VCC-VC) is higher than the Overcharge Detection Threshold Voltage (VCT), or the VC is higher than the Cell-balance 2 Threshold (Vbal2), the bypass balance circuit is switched off by the P-MOSFET.

As the same, when the VC is between the Cell-balance 2 Threshold (VBAL2) and the Overcharge Detection Threshold Voltage (VCT), and (VCC-VC) is below the Cell-balance 1 Threshold (VBAL1) for the Cell-balance 2 Detection Delay Time(T_{BAL2}) or longer, the Bal2 pin controls the N-MOSFET to switch on the other bypass balance circuit. When the VC is higher than the Overcharge Detection Threshold Voltage (VCT) or the (VCC-VC) is higher than the Cell-balance Threshold 1(VBAL1), the bypass balance circuit is switched off by the N-MOSFET.

10. Abnormal Charge Current Condition:

If the VM pin voltage falls below the Abnormal Charge Current Detection Threshold Voltage (VAB) during charging under normal condition and takes the Abnormal Charge Current Detection Delay Time (T_{AB}) or longer, the charging control FET is turned off and charging stops. This action is called the Abnormal Charge Current Detection. Abnormal charge current detection works when the DO pin voltage is “H” and the VM pin voltage falls below the Abnormal Charge Current Detection Threshold Voltage (VAB). To an over-discharged battery, only when charging makes the battery voltage higher than the Over-discharge Detection Threshold (VDT), the Abnormal Charge Current Detection can act. Abnormal charge current state is released, once the voltage difference between VM pin and VSS pin becomes less than the Abnormal Charge Current Detection Threshold Voltage (VAB) value.

11. Charger Detect Condition:

A two-cell battery in over-discharge condition can be released, when it is connected to a charger, the VM pin voltage is lower than the Abnormal Charge Current Detection Threshold Voltage (VAB), and each cell voltage becomes higher than the Over-discharge Detection Threshold Voltage (VDT). This action is called Charger Detection. But, if the VM pin voltage is between the Abnormal Charge Current Detection Threshold Voltage (VAB) and the Excess Current 1 Detection Threshold Voltage (VIT1), the over-discharge state is not released unless the two cell voltages both become higher than the Over-discharge Release Voltage (VDR).

Electrical Characteristic [1*]

(T_{OPT}=25℃ unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Circuit
Detection Voltage and Delay Time (C_4=0.01u F)							
Overcharge Detection Voltage 1,2	VCT1,2 [2*]	25℃	VCT1,2-0.050	VCT1,2	VCT1,2+0.050	V	1
Overcharge Release Voltage 1,2	VCR1,2 [3*]	25℃	*VCT1,2* - 0.40	*VCT1,2* -0.3	*VCT1,2* - 0.20	V	1
Over-discharge Detection Voltage 1,2	VDT1,2 [2*]	25℃	VDT1,2- 0.08	VDT1,2	VDT1,2 + 0.08	V	1
Over-discharge Release Voltage 1,2	VDR1,2 [3*]	25℃	*VDT1,2* + 0.55	*VDT1,2*+0.7	*VDT1,2* + 0.85	V	1
Excess Current 1 Detection Voltage	VIT1	V1=V2 =2.85V	0.18	0.20	0.22	V	1
Excess Current 2 Detection Voltage	VIT2	V1=V2 =2.85V	0.50	0.60	0.70	V	1
Short Circuit Detection Voltage	VSHORT	V1=V2 =2.85V	1	1.50	2	V	1
Cell-balance 1 Threshold	VBAL1	25℃	3.52	3.62	3.72	V	1
Cell-balance 2 Threshold	VBAL2	25℃	3.52	3.62	3.72	V	1
Abnormal Charge Detection Voltage	VAB	V1=V2 =2.85V	-0.17	-0.15	-0.13	V	1
Charger Detection Voltage	VCHA	V1=V2 =2.85V	-0.17	-0.15	-0.13	V	1
Overcharge Detection Delay Time	T_{CT}	V1=V2 =3.90V	42	85	170	ms	3
Over Discharge Detection Delay Time	T_{DT}	V1=V2 =1.80V	12	24	48	ms	3
Excess Current 1 Detection Delay Time	T_3	V1=V2 =2.85V	6	12	24	ms	3
Excess Current 2 Detection Delay Time	T_4	V1=V2 =2.85V	1	2	3	ms	3
Short Circuit Detection Delay Time	T_5	V1=V2=2.85V			10	us	3
Abnormal Charge Detection Delay Time	T_{AB}	V1=V2=2.85V	42	85	170	ms	3
Cell-balance 1 Detection Delay Time	T_{BAL1}	V1=3.75V V2=3.30V	3	5	10	ms	3
Cell-balance 2 Detection Delay Time	T_{BAL2}	V1=3.30V V2=3.75V	3	8	15	ms	3
Output Voltage And VM Internal Resistance							
CO "H" Voltage	VCO(H)	V1=V2=3.40V	6.55	6.60		V	4
CO "L" Voltage	VCO(L)	V1=V2=4V		0.10	0.13	V	4
DO "H" Voltage	VDO(H)	V1=V2=3.40V	3.27	3.32		V	4
DO "L" Voltage	VDO(L)	V1=V2=1.80V		0.05	0.08	V	4
Resistance Between VM And VCC	R_{VMD}	V1=V2=1.80V VM=0V	40	110	200	KΩ	4
Resistance Between VM And VSS	R_{VMS}	V1=V2=2.85V VM=1V	50	150	300	KΩ	4
Operation Voltage And Current Consumption							
Operation Voltage Between VCC And VSS	VCSOP	25℃	2	-	16	V	
Operation Voltage Between VCC And VM	VCMOP	25℃	5	-	28		
Current Consumption During Normal State	I_{OPE}	V1 = V2 = 3.30V	5	10	150	uA	2
Current Consumption During Power Down	I_{PDN}	V1 = V2 = 1.80V	0.50	0.90	1.50	uA	2

1* The Electrical parameters for this temperature range is guaranteed by design, not tested in production.

2* See "Selection Guide" section.

3* *VCT1,2* and *VDT1,2* are the Overcharge and Over-discharge threshold voltage of actual testing.

4* V1 is the voltage of cell1 and V2 is the voltage of cell2, refer to the Typical Application Circuits and test circuits.

Electrical Characteristic [1*]

(T_{OPT}=-20~70℃ unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Circuit
Detection Voltage							
Overcharge Detection Voltage 1,2	VCT1,2 [2*]		VCT1,2-0.080	VCT1,2	VCT1,2+0.080	V	1
Overcharge Release Voltage 1,2	VCR1,2 [3*]		*VCT1,2* -0.45	*VCT1,2* -0.3	*VCT1,2* -0.15	V	1
Over-discharge Detection Voltage 1,2	VDT1,2 [2*]		VDT1,2- 0.10	VDT1,2	VDT1,2 + 0.10	V	1
Over-discharge Release Voltage 1,2	VDR1,2 [3*]		*VDT1,2* + 0.50	*VDT1,2*+0.7	*VDT1,2* + 0.90	V	1
Excess Current 1 Detection Voltage	VIT1	V1=V2 =2.85V	0.17	0.20	0.23	V	1
Excess Current 2 Detection Voltage	VIT2	V1=V2 =2.85V	0.40	0.60	0.8	V	1
Short Circuit Detection Voltage	VSHORT	V1=V2 =2.85V	1	1.50	2	V	1
Cell-balance 1 Threshold	VBAL1	25℃	3.47	3.62	3.77	V	1
Cell-balance 2 Threshold	VBAL2	25℃	3.47	3.62	3.77	V	1
Abnormal Charge Detection Voltage	VAB	V1=V2 =2.85V	-0.18	-0.15	-0.12	V	1
Charger Detection Voltage	VCHA	V1=V2 =2.85V	-0.18	-0.15	-0.12	V	1
Overcharge Detection Delay Time	T_{CT}	V1=V2 =3.90V	30	85	200	ms	3
Over Discharge Detection Delay Time	T_{DT}	V1=V2 =1.80V	8	24	60	ms	3
Excess Current 1 Detection Delay Time	T_3	V1=V2 =2.85V	4	12	30	ms	3
Excess Current 2 Detection Delay Time	T_4	V1=V2 =2.85V	1	2	5	ms	3
Short Circuit Detection Delay Time	T_5	V1=V2=2.85V			10	us	3
Abnormal Charge Detection Delay Time	T_{AB}	V1=V2=2.85V	8	85	200	ms	3
Cell-balance 1 Detection Delay Time	T_{BAL1}	V1=3.75V V2=3.3V	3	5	12	ms	3
Cell-balance 2 Detection Delay Time	T_{BAL2}	V1=3.30V V2=3.75V	3	8	20	ms	3
Output Voltage And VM Internal Resistance							
CO "H" Voltage	VCO(H)	V1=V2=3.40V	6.50	6.60		V	4
CO "L" Voltage	VCO(L)	V1=V2=4V		0.10	0.15	V	4
DO "H" Voltage	VDO(H)	V1=V2=3.40V	3.22	3.32		V	4
DO "L" Voltage	VDO(L)	V1=V2=1.80V		0.05	0.10	V	4
Resistance Between VM And VCC	R_{VMD}	V1=V2=1.80V VM=0V	30	110	250	KΩ	4
Resistance Between VM And VSS	R_{VMS}	V1=V2=2.85V VM=1V	40	150	400	KΩ	4
Operation Voltage And Current Consumption							
Operation Voltage Between VCC And VSS	VCSOP		2	-	16	V	
Operation Voltage Between VCC And VM	VCMOP		5	-	28		
Current Consumption During Normal State	I_{OPE}	V1 = V2 = 3.30V	5	10	18	uA	2
Current Consumption During Power Down	I_{PDN}	V1 = V2 = 1.80V	0.50	0.90	1.50	uA	2

1* The Electrical parameters for this temperature range is guaranteed by design, not tested in production.

2* See "Selection Guide" section.

3* *VCT1,2* and *VDT1,2* are the Overcharge and Over-discharge threshold voltage of actual testing.

4* V1 is the voltage of cell1 and V2 is the voltage of cell2, refer to the Typical Application Circuits and test circuits.

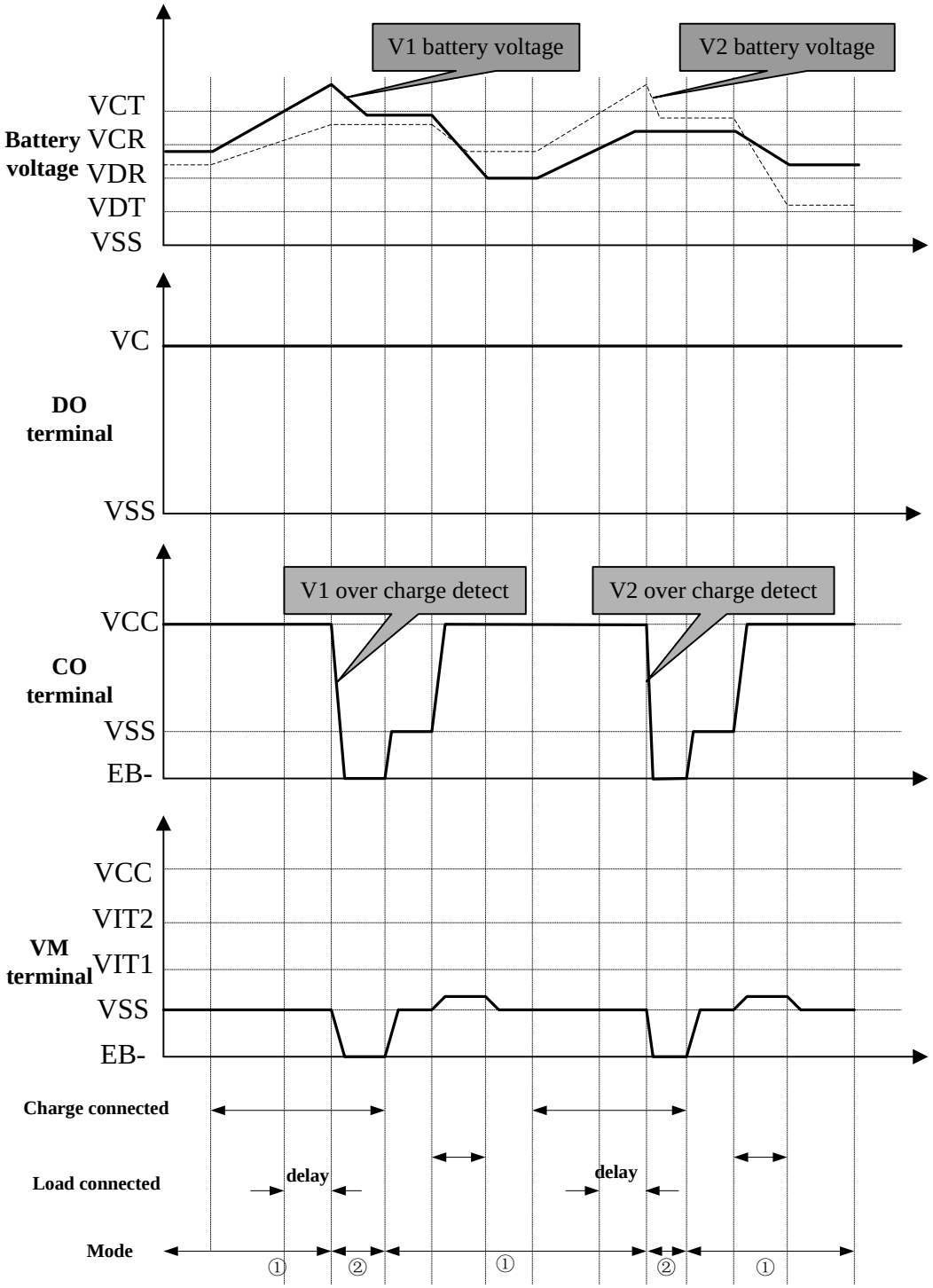
Absolute Maximum Ratings

Item	Symbol	Pin	Rated Value	Unit
VCC-VSS Input Voltage	V_{DSH}	VCC	VSS-0.30~VSS+18	V
VC-VSS Input Voltage	V_{DSL}	VC	VSS-0.30~VSS+7.0	V
Sense Pin Input Voltage	V_{Sense}	Sense	VSS-0.30~VCC+0.30	V
Delay Pin Input Voltage	V_{CT}	CT	VSS-0.30~VC+0.30	V
VM Pin Input Voltage	V_{VM}	VM	VCC-28~VCC+0.30	V
DO Pin Output Voltage	V_{DO}	DO	VSS-0.30~VC+0.30	V
CO Pin Output Voltage	V_{CO}	CO	VM-0.30~VCC+0.30	V
Bal1 Pin Output Voltage	V_{Bal1}	Bal1	VSS-0.30~VC+0.30	V
Bal2 Pin Output Voltage	V_{Bal2}	Bal2	VSS-0.30~VC+0.30	V
Power Dissipation	P_D	-----	300	mW
Operation Temperature	T_{opr}	-----	-20~+85	℃
Storage Temperature	T_{stg}	-----	-40~+125	℃

Attention: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

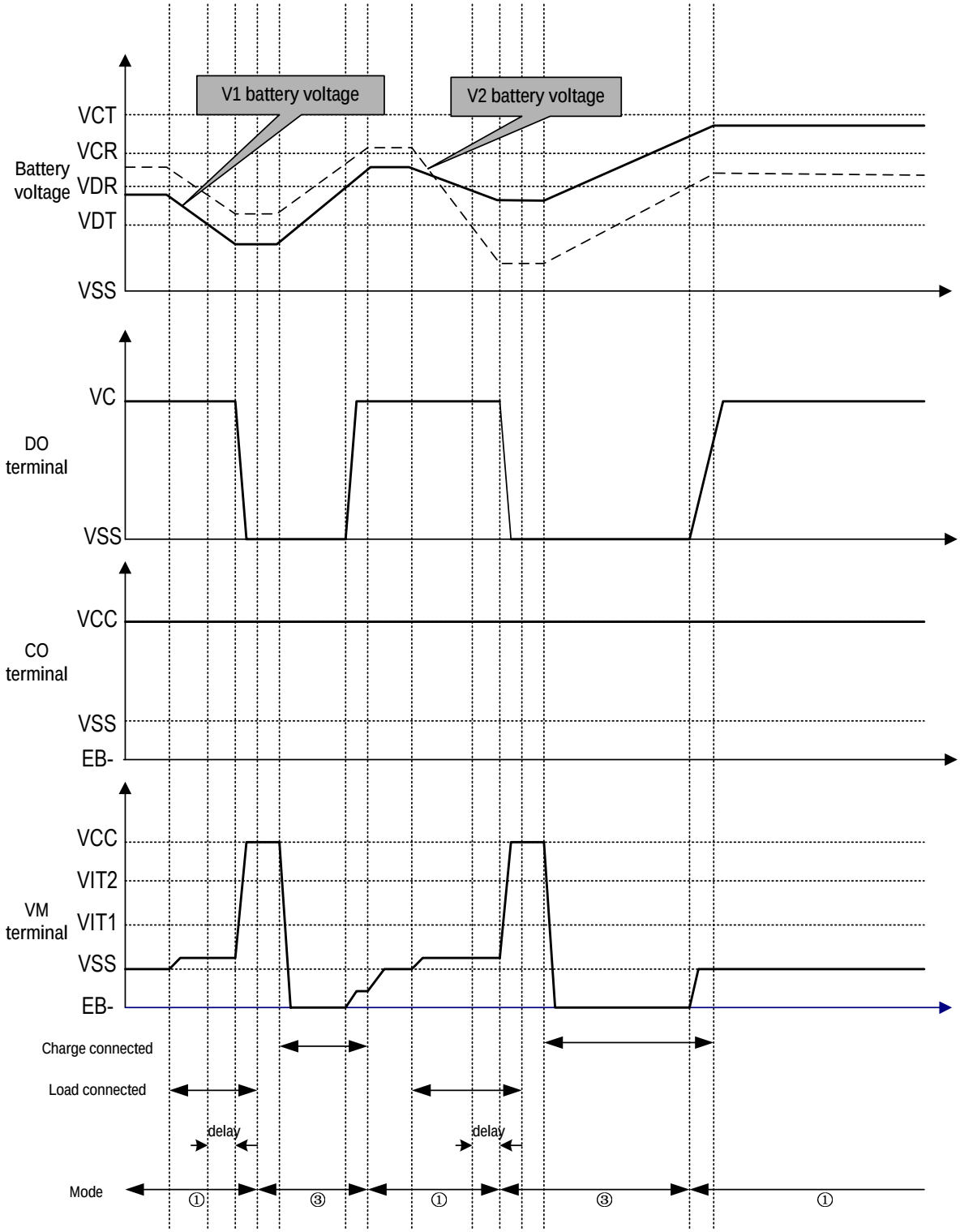
Operation Timing Charts:

Overcharge:



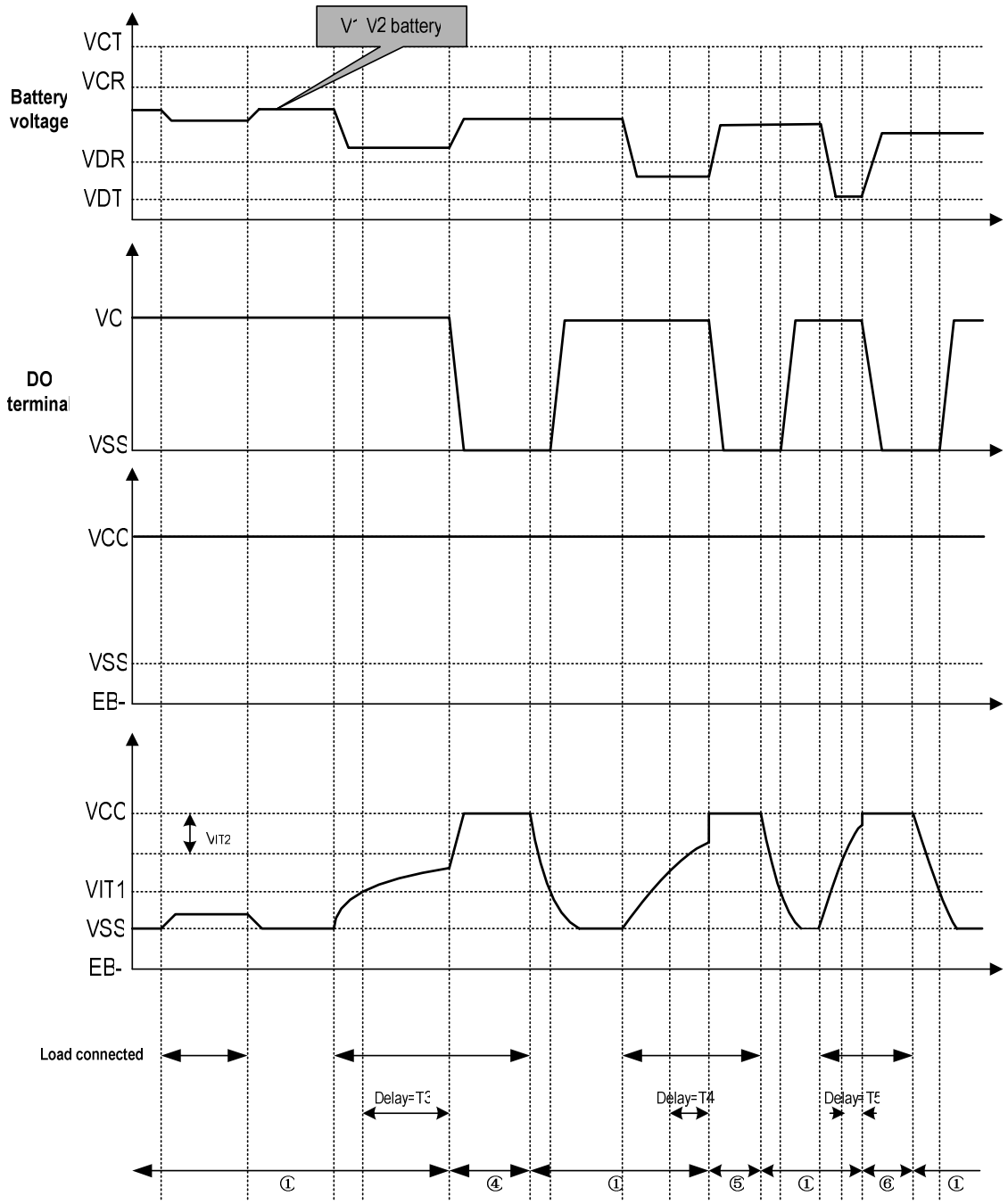
Note: ① Normal mode ② Overcharge mode ③ Over-discharge mode
④ Excess current 1 mode ⑤ Excess current 2 mode
⑥ Short circuit mode ⑦ Bypass current work mode
The number N = the times of the charge-discharge cycle.

Over-discharge：



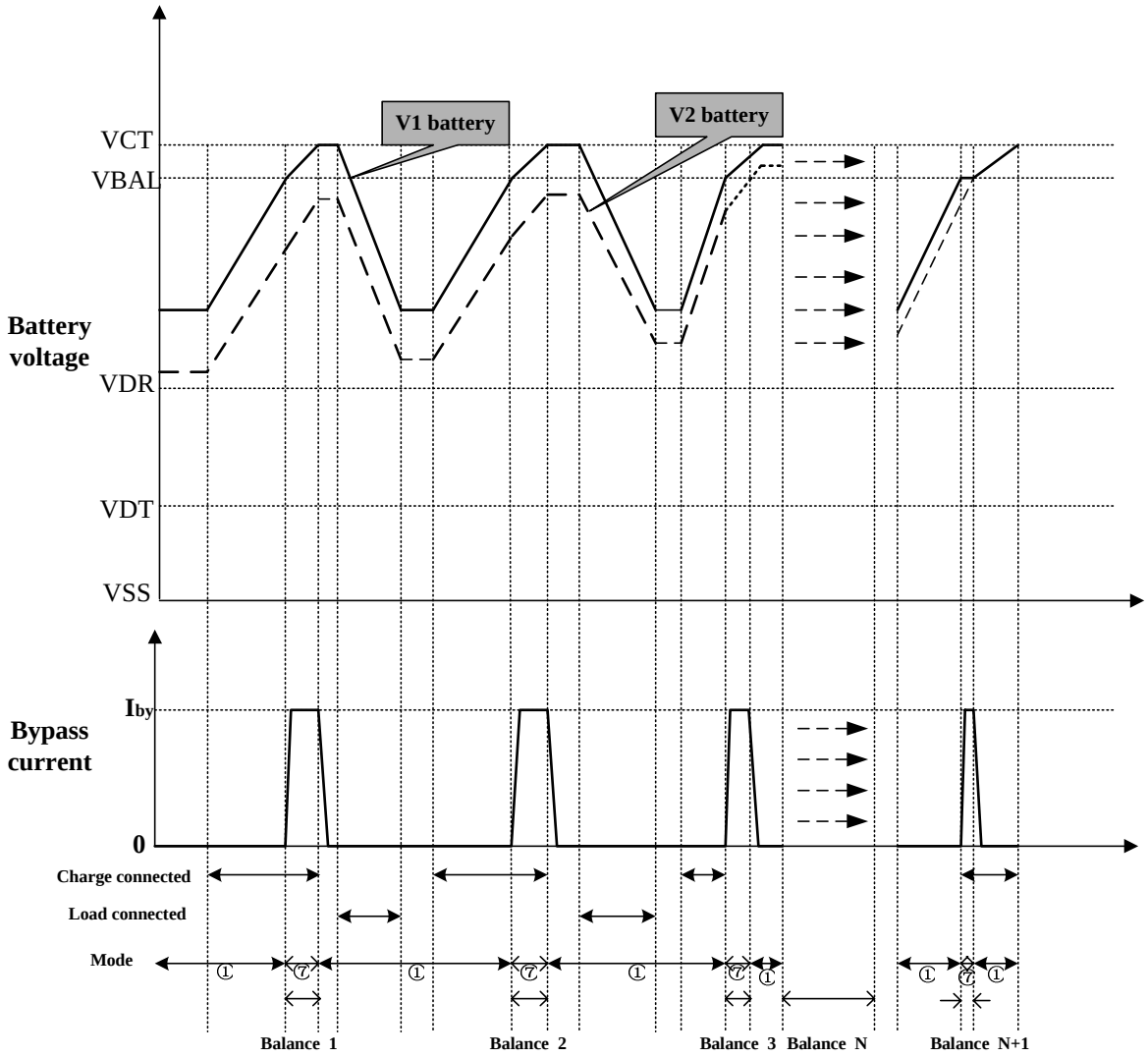
Note: ① Normal mode ② Overcharge mode ③ Over-discharge mode
④ Excess current 1 mode ⑤ Excess current 2 mode
⑥ Short circuit mode ⑦ Bypass current work mode
The number N = the times of the charge-discharge cycle.

Excess current:



Note: ① Normal mode ② Overcharge mode ③ Over-discharge mode
④ Excess current 1 mode ⑤ Excess current 2 mode
⑥ Short circuit mode ⑦ Bypass current work mode
The number N = the times of the charge-discharge cycle.

Cell-balance Function:



Note: ① Normal mode ② Overcharge mode ③ Over-discharge mode
④ Excess current 1 mode ⑤ Excess current 2 mode
⑥ Short circuit mode ⑦ Bypass current work mode
The number N = the times of the charge-discharge cycle.

Test Circuits

(1) Overcharge detection threshold voltage and overcharge release voltage

Test circuit 1

Set V2=3.30V V3=0V, the Overcharge Detection Threshold Voltage (VCT1) is the voltage between VCC and VC to which when V1 increases and keeps the condition for the Overcharge Detection Delay Time (T_{CT}), VCO changes from "H" to "L". The overcharge release voltage (VCR1) is the voltage between VCC and VC to which when V1 decreases, VCO changes from "L" to "H".

Set V1=3.30V V3=0V, the Overcharge Detection Threshold Voltage (VCT2) is the voltage between VC and VSS to which when V2 increases and keeps the condition for the Overcharge Detection Delay Time (T_{CT}), VCO changes from "H" to "L". The Overcharge Release Voltage (VCR2) is the voltage between VC and VSS to which when V2 decreases, VCO changes from "L" to "H".

(2) Over-discharge detection threshold voltage and over-discharge release voltage

Test circuit 1

Set V2=3.30V V3=0V, the Over-discharge Detection Threshold Voltage (VDT1) is the voltage between VCC and VC to which when V1 decreases and keep the condition for the Over-discharge Detection Delay Time (T_{DT}), VDO changes from "H" to "L". The Over-discharge Release Voltage (VDR1) is the voltage between VC and VSS to which when V1 increases, VDO changes from "L" to "H".

Set V1=3.30V V3=0V, the Over-discharge Detection Threshold Voltage (VDT2) is the voltage between VC and VSS to which when V2 decreases and keep the condition for the Over-discharge Detection Delay Time (T_{DT}), VDO changes from "H" to "L". The Over-discharge Release Voltage (VDR2) is the voltage between VC and VSS to which whenV2 increases, VDO changes from "L" to "H".

(3) Excess current detection threshold voltage and short circuit detection threshold voltage

Test circuit 1

Set V1=V2=2.85V, the Excess Current 1 Detection Threshold Voltage (VIT1) is the voltage V3 between VM and VSS to which when VM increases within 10 us and keep the condition for the Excess Current 1 Detection Delay Time (T_3), VDO changes from "H" to "L".

The Excess Current 2 Detection Threshold Voltage (VIT2) is the voltage V3 between VM and VSS to which when VM increases within 10 us and keep the condition for the Excess Current 2 Detection Delay Time (T_4), VDO changes from "H" to "L".

The Short Circuit Detection Threshold Voltage (V_{SHORT}) is the voltage V3 between VM and VSS to which when VM increases within 10us and keep the condition for the Short Circuit Detection Delay Time (T_5), VDO changes from "H" to "L".

(4) Charger detection threshold voltage and abnormal charge current detection threshold voltage

Test circuit 1

In the over-discharge condition, increase V2 gradually until it is between VDT2 and VDR2. The voltage between VM and VSS to which when V3 decreases from 0V, VDO changes from "L" to "H", is the Charger Detection Threshold Voltage (VCHA).

In the normal charging condition, the voltage between VM and VSS to which when V3 decreases from 0V, VCO changes from "H" to "L" is the Abnormal Charge Current Detection Threshold Voltage (VAB). It has the same value as the Charger Detection Threshold Voltage (VCHA).

(5) Normal operation current consumption and power down current consumption

Test circuit 2

Set V1=V2=3.30V, the current A1 flowing through VCC and Sense pin and the current A2 flowing through VC pin are the normal operation consumption current (I_{OPE}).

Set V1=1.80V V2=1.80V, the current A1 flowing through VCC and Sense pin and the current A2 flowing through VC pin are the power down current consumption (I_{PDN}).

(6) Overcharge detection delay time and over-discharge detection delay time

Test circuit 3

Set V3=0V, If V1 or V2 increases to be VCT1 or over VCT1 and keeps the condition for some time, VCO will change from "H" to "L". The time is called Overcharge Detection Delay Time (T_{CT}). It is used to judge whether overcharge

happens indeed.

Test circuit 3

Set V3=0V, If V1 or V2 decreases to be VDT1 or below VDT1 and keeps the condition for some time, VDO will change from “H” to “L”. The time is called Over-discharge Detection Delay Time (T_{DT}). It is used to judge whether over-discharge happens indeed.

(7) Excess current detection delay time and short circuit detection delay time

Test circuit 3

Set V1=V2=2.85V, If V3 increases to be VIT1 or over VIT1 and keeps the condition for some time, VDO will change from “H” to “L”. The time is called Excess Current 1 Detection Delay Time (T_3). It is used to judge whether excess current 1 happens indeed.

Set V1=2.85V V2=2.85V, If V3 increases to be VIT2 or over VIT2 and keeps the condition for some time, VDO will change from “H” to “L”. The time is called Excess Current 2 Detection Delay Time (T_4). It is used to judge whether excess current 2 happens indeed.

Set V1=2.85V V2=2.85V, If V3 increases to be VSHORT or over VSHORT and keeps the condition for some time, VDO will change from “H” to “L”. The time is called Short Circuit Delay Time (T_5). It is used to judge whether short circuit happens indeed.

(8) Cell-balance threshold

Test Circuit 1

Set V2=3.30V V3=0V, the Cell-balance1 threshold (VBAL1) is the voltage between VCC and VC to which when V1 increases and keeps the condition for Cell-balance 1 Detection Delay Time (T_{BAL1}), V_{Bal1} changes from “H” to “L”.

Set V1=3.30V V3=0V, the overcharge detection voltage (VCT2) is the voltage VC which when V2 increases and keeps the condition for Cell-balance Detection 2 Delay Time (T_{BAL2}), VBal2 changes from “L” to “H”.

(9) Cell-balance Detection Delay Time

Test Circuit 3

Set V2=3.30V V3=0V, If V1 increases to be VBAL1 or over VBAL1 but lower than VCT1 and keeps the condition for some time, V_{Bal1} will change from “H” to “L”. The time is called cell-balance 1 detection delay time. It is used to judge whether a bypass balance current is need indeed.

Set V1=3.30V V3=0V, If V2 increases to be VBAL2 or over VBAL2 but lower than VCT2 and keeps the condition for some time, V_{Bal2} will change from “L” to “H”. The time is called cell-balance 2 detection delay time. It is used to judge whether a bypass balance current is need indeed.

(10) CO and DO output voltage

Test Circuit 4

Set V1=V2=3.40V, V5=0V, K1 on and K2 off, increaseV4 from 0V gradually, the V4 voltage when A2 = 50uA is the CO 'H' voltage (VCOH).

Set V1=V2=4V, V5=0V, K1 on and K2 off, increase V4 from 0V gradually, the V4 voltage when A2 = – 50uA is the CO 'L' voltage (VCOL).

Set V1=V2=3.40V, V5=0V, K1 off and K2 on, increase V3 from 0V gradually, the V3 voltage when A1 = 50uA is the DO 'H' voltage (VDOH).

Set V1=V2=1.80V, V5=0V, K1 off and K2 on, increase V3 from 0V gradually, the V3 voltage when A1= – 50uA is the DO 'L' voltage (VDOL).

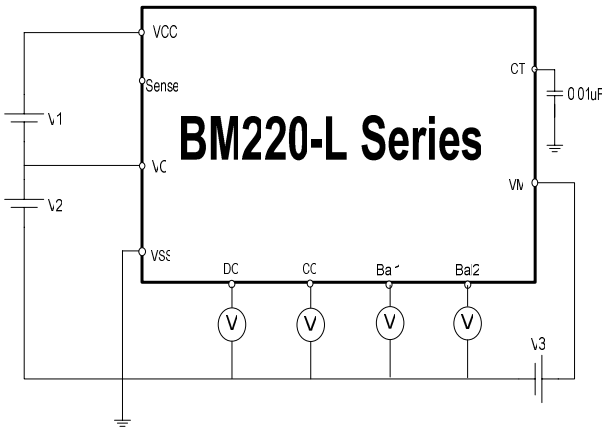
(11) Internal resistance VM–VCC and VM-VSS

Test circuit 4

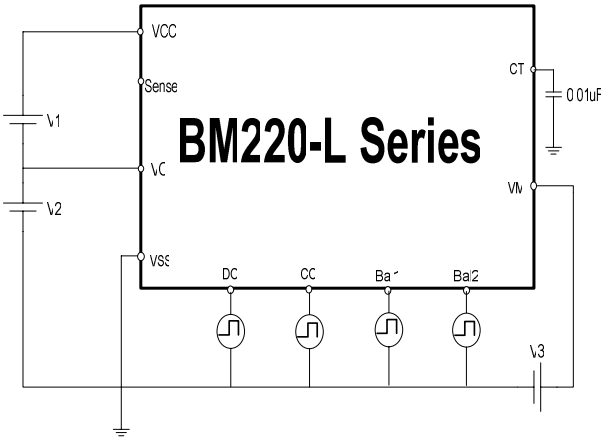
Set V1=V2=1.80V, V5=0V, K1 off and K2 off, (V1+V2)/I3 is the internal resistance $R_{VMD.}$

Set V1=V2=2.85V, V5=1V, K1 off and K2 off, V5/I3 is the internal resistance $R_{VMS.}$

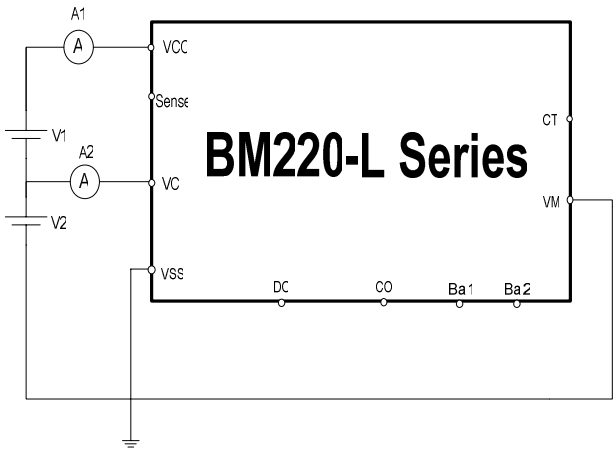
Test Circuits



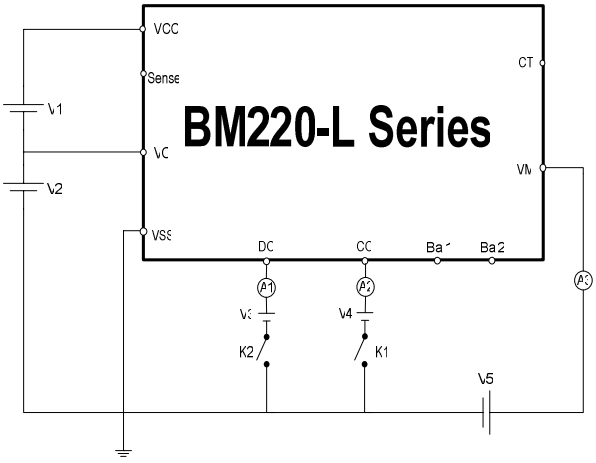
Circuit1



Circuit3

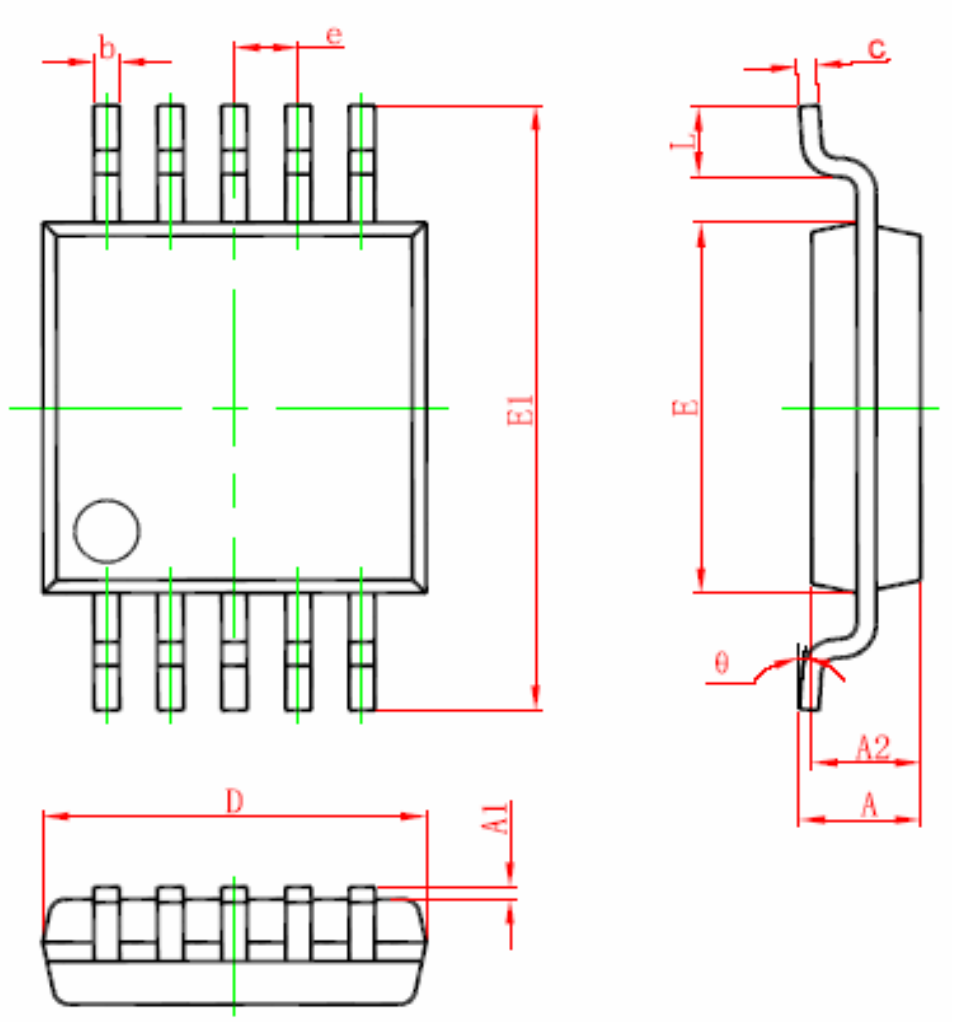


Circuit2



Circuit4

Package Outline



Dimensions **UNIT (mm)**

	A	A1	A2	b	c	D	e	E	E1	L	θ
Min.	0.820	0.020	0.750	0.180	0.090	2.900	0.50 BSC	2.900	4.750	0.400	0°
Max.	1.100	0.150	0.950	0.280	0.230	3.300		3.300	5.050	0.800	6°

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